PATENT ABSTRACTS

[** your application **]

6/5/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014742485 & & *Drawing available*
WPI Acc no: 2005-090111/200510
XRPX Acc No: N2005-078791
Logical partition application amount usage determining method for use in computer system, involves determining bill for each application by billing function based on usage amount of each application
Patent Assignee: MATHIAS T B (MATH-I); NECHEMIAS M J (NECH-I); TINGEY M O (TING-I); WASSEL P S (WASS-I)
Inventor: MATHIAS T B; NECHEMIAS M J; TINGEY M O; WASSEL P S

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050004879	A1	20050106	US 2003613779	A	20030701	200510	B

Priority Applications (no., kind, date): US 2003613779 A 20030701

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050004879	A1	EN	18	10	

Alerting Abstract US A1
NOVELTY - The method involves determining information indicative of an amount of usage of each application by guest operating system or other program executing in a logical partition (LPAR). An amount of usage of each application is reported to a billing function based on the information. A bill for each of the application is determined by a billing function based on the amount of usage of each application.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

a. a system of determining an amount of usage of applications in an LPAR in a computer system and a bill for such usage
b. a computer program product for determining an amount of usage of applications in an LPAR in a computer system and a bill for such usage.

USE - Used for determining an amount of usage of an application in a logical partition (LPAR) of a computer system for billing the usage.
ADVANTAGE - The method enables a system administrator to easily determine the amount of usage of the applications in the logical partition, and to bill the usage
DESCRIPTION OF DRAWINGS - The drawing shows a flow chart illustrating an application usage metering function within a guest operating system of a computer system.

11/5/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0009219000 & & *Drawing available*
WPI Acc no: 1999-145154/199913
XRPX Acc No: N1999-105682
Multiple logical channel charging method for limiting internet congestion
Patent Assignee: AT & T CORP (AMTT)
Inventor: ODLYZKO A M

Patent Family (4 patents, 27 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 899916	A2	19990303	EP 1998306348	A	19980807	199913	B
CA 2244569	A	19990207	CA 2244569	A	19980807	199930	E
US 6295294	B1	20010925	US 1997908689	A	19970807	200158	E
CA 2244569	C	20040406	CA 2244569	A	19980807	200425	E

Priority Applications (no., kind, date): US 1997908689 A 19970807

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 899916	A2	EN	10	3		
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
CA 2244569	A	EN				
CA 2244569	C	EN				

Alerting Abstract EP A2
NOVELTY - The communication system, e.g. internet, has many users communicating over the network and causing congestion. The system creates a number of logical channels through the network that represent a priority of service, i.e. higher priority receives higher throughput. The user is allowed to select a priority channel and is charged for the extent of use of that channel. Higher priority channels have higher charges hence causing a user to make balanced use of the network.
DESCRIPTION - INDEPENDENT CLAIMS are included for a regulated packet switched network and a method of limiting congestion
USE - In networks suffering from congestion.
ADVANTAGE - Provides incentives for users to balance their communications and to Service providers to provide better services.
DESCRIPTION OF DRAWINGS - The drawing shows a schematic of a network communication.
10 User
30 Congested network
40 Router implementing priority channels
50-54 Other users

15/5/7 (Item 7 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0012759731 & & *Drawing available*
WPI Acc no: 2002-613277/200266
XRPX Acc No: N2002-485793
Logic partition-type calculator manages utilization of same information between logic compartments by operation of software in logic compartments
Patent Assignee: HITACHI LTD (HITA)
Inventor: MIYATA K; OCHIAI N

Patent Family (2 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 2002215407	A	20020802	JP 200112609	A	20010122	200266	B
JP 3879405	B2	20070214	JP 200112609	A	20010122	200714	E

Priority Applications (no., kind, date): JP 200112609 A 20010122

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
JP 2002215407	A	JA	7	7		
JP 3879405	B2	JA	8		Previously issued patent	JP 2002215407

Alerting Abstract JP A
NOVELTY - A controller (5) assign a main memory area to a logic compartment (3a) which is referred from other logic compartment (3b). The controllers (7a,7b) manages utilization of the same information between the logic compartments by the operation of the software in the logic compartments, as the main memory area is referred from the other logic compartment.
USE - Logic partition-type calculator.
ADVANTAGE - The change of the software is performed safely and inexpensively without stopping the work of the system.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the logic partition-type calculator. (Drawing includes non-English language text).
3a,3b Logic compartments
5 Controller
7a,7b Controllers

19/5/5 (Item 5 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014020708 & & *Drawing available*
WPI Acc no: 2004-202401/200419
XRPX Acc No: N2004-160916
Server for fiber channel communication, has adapter component for receiving request from operating system and assigning access rights to system, and fiber channel PCI adaptor to send request to resource via fiber channel
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ADLUNG I; BANZHAF G; ECKERT W; LAMBERTZ K; MUELLER S; RAISCH C

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040025166	A1	20040205	US 2003353743	A	20030129	200419	B

Priority Applications (no., kind, date): EP 20022496 A 20020202

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20040025166	A1	EN	7	2	

Alerting Abstract US A1
NOVELTY - The server has an adapter component (6) for receiving a request from an operating system of server. The component has an administration module (7) for assigning of access rights to the system. The request is granted in case of compliance with the corresponding rights. A fiber channel PCI adaptor serves as a common access point of the server and a fiber channel sends the request to a resource via the channel (15).
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

c. a method for accessing a resource from a virtual machine provided by a server computer
d. a computer program product for accessing a resource from a virtual machine.

USE - Used in a fiber channel communication.
ADVANTAGE - The same fiber channel adapter can be used by a number of virtual machines for sharing of system resources over the fiber channel. The billing for leasing or renting of the virtual machine depends on the extent of access rights being granted to the machine, thereby allowing to independently rent or lease the machines on the server.
DESCRIPTION OF DRAWINGS - The drawing shows a block diagram of a computer system.
1Server computer
6Adapter component
7Access rights administration module
14Fiber channel PCI adapter
15Fiber channel

22/5/9 (Item 8 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0009814682 & & *Drawing available*
WPI Acc no: 2000-104991/200009
XRPX Acc No: N2000-080643
Distributed applications processing device with host coupled to peripheral device using network
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: GAO J; PELISSIER G; YAN A

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6003065	A	19991214	US 1997845564	A	19970424	200009	B

Priority Applications (no., kind, date): US 1997845564 A 19970424

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 6003065	A	EN	104	4	

Alerting Abstract US A
NOVELTY - A host (102A) selects particular peripheral device (102B-102G) which should execute an application with a virtual machine instruction. A download mechanism transfers the application to the selected peripheral device. The peripheral device has a virtual machine instruction processor that executes a portion of the application including the virtual machine instruction.
DESCRIPTION - The host computer has a network interface coupled to network for bidirectional transmission of data between host computer and network. A storage device stores the application. The peripheral device has another network interface coupled to the network. The peripheral devices included in database (110) includes printed devices. A predetermined criteria is used to select the peripheral device, including cost, speed, quality, performance etc.
An INDEPENDENT CLAIM is also included for method of distributing the processing of application.
USE - For distributed processing of applications, with host computer coupled by network to peripheral devices, for use in business organization, for distribution of processing over Internet and Intranet.
ADVANTAGE - Executables running on host device are also efficiently downloaded and executed efficiently on target peripheral device. Executables are shared, thus opening up robust communication between the peripheral device and host machine. Results in lower total cost of operation and ownership because peripheral devices can be managed more easily and efficiently. The distributed data processing system based on peripheral devices presents attractive price for performance characteristics.
DESCRIPTION OF DRAWINGS - The figure shows the computer network.
102A Host computer
102B-102G Peripheral devices
110 Database

FULL-TEXT PATENTS

6/3K/1 (Item 1 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

00985859
METHOD FOR PRICING ACCESS TO A PLURALITY OF SOFTWARE PROGRAMS
PROCEDE PERMETTANT D'ETABLIR LE PRIX D'UN ACCES A UNE PLURALITE DE PROGRAMMES LOGICIELS

Patent Applicant/Patent Assignee:

e. ASG INC; 1333 South Third Avenue, Naples, FL 34102
US; US(Residence); US(Nationality)

Legal Representative:

f. HUANG Stuart T F(et al)(agent)
Steptoe & Johnson LLP, 1330 Connecticut Avenue, N.W., Washington, DC 20036; US;

	Country	Number	Kind	Date
Patent	WO	200314869	A2-A3	20030220
Application	WO	2002US24361		20020802
Priorities	US	2001920617		20010803

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LU; MC; NL; PT;
SE; SK; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;

[AP] GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ;
UG; ZM; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 4128

Detailed Description:

...to at least one of the current capacity and the future capacity. The determining a price preferably reflects an inverse relationship between the cost-per-unit capacity and the appropriate capacity, or, when the appropriate capacity exceeds a threshold value, the determining a price reflects an inverse relationship between the cost-per-unit capacity and the appropriate capacity. The determining a price preferably includes one of the mathematical processing of the appropriate capacity, and a modification of...access to

the plurality of computer programs, but not to individual ones of the computer programs, determining a use fee to use one of the individual computer programs over a period of time based... ...the one of the individual computer programs is resident.

The sub-section is preferably a logical partition of the site or a collection of the 1 5 individual computers on which the...a current capacity of the site and a future capacity of the site, determining a price at least partially from at least one of mathematical processing of at least the appropriate...capacity and a period of time of desired access, and receiving compensation consistent with the price, and providing access to any of the plurality of computer programs.

According to various preferably... ...to the - 3 plurality of computer programs, but not to individual ones of the computer programs, and determining a use fee to use one of the individual computer programs over a period of time based...the one of the individual computer programs is resident. The sub-section is preferably a logical partition of the site or a collection of the individual computers on which the one of the individual computer programs is resident.

The determining a price preferably reflects an inverse relationship between the cost-per-unit capacity and the appropriate capacity, or, when the appropriate capacity exceeds a threshold value, the determining a price preferably reflects an inverse 1 0 relationship between the cost per unit capacity and the...

Claims:

...capacity and the future capacity.

11 The method of claim 8, wherein said determining a price reflects an
inverse relationship between the cost-per-unit capacity and the appropriate capacity.
12... ...of claim 8 wherein when said appropriate capacity exceeds
a threshold value, said determining a price reflects an inverse relationship between the cost-per-unit capacity and the appropriate capacity. - I I . The method of claim 8, said determining a price comprising one of themathematical processing of the appropriate capacity, and a modification of the...access to the plurality of computer programs, but not to individual ones of the computer programs; and determining a use fee to use one of the individual computer programs over a period of time based... ...programs is resident.
15 The method of claim 14, wherein said sub-section is a logical partition of the site.

16 The method of claim 14, wherein said sub-section is a...a current capacity of the site and a future capacity of the
site;determining a price at least partially from at least one of:mathematical processing of at least the appropriate...capacity and a period of time of desired access; andreceiving compensation consistent with the price; andproviding access to any of said plurality of computer programs.
18 The method of... ...access to the plurality of computer programs, but not to individual ones of the computer programs; determining a use fee to use one of the individual computer programs over a period of time based ...programs is resident.

19 The method of claim 18, wherein said sub-section is a logical partition of the site.

20 The method of claim 18, wherein said sub-section is a... ...k and z are variables.

22 The method of claim 17, wherein said determining a price reflects an
inverse relationship between the cost-per-unit capacity and the appropriate capacity. -

[**bad date?**]

14/3K/7 (Item 2 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

01165524
METHOD TO PROVIDE ON-DEMAND RESOURCE ACCESS
PROCEDE POUR FOURNIR UN ACCES A DES RESSOURCES SUR DEMANDE

Patent Applicant/Patent Assignee:

g. INTERNATIONAL BUSINESS MACHINES CORPORATION; New Orchard Road, Armonk, New York 10504
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(For all designated states except: US)

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j. GRIMM Randall Lane; 5811 Colonial Lane S.E, Rochester, Minnesota 55904
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(Designated only for: US)

k. LEWIS David Otto; 1609 Ridge Drive N.E, Rochester, Minnesota 55906
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(Designated only for: US)

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Patent Applicant/Inventor:

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(Designated only for: US)

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(Designated only for: US)

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1083 White Birch Court N.W, Oronoco, Minnesota 55960; US; US(Residence); US(Nationality);
(Designated only for: US)

Legal Representative:

q. MATHER Belinda(agent)
IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester, Hampshire SO21 2JN; GB;

	Country	Number	Kind	Date
Patent	WO	200488506	A2-A3	20041014
Application	WO	2004GB1219		20040322
Priorities	US	2003406652		20030403

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG;
BR; BW; BY; BZ; CA; CH; CN; CO; CR; CU;
CZ; DE; DK; DM; DZ; EC; EE; EG; ES; FI;
GB; GD; GE; GH; GM; HR; HU; ID; IL; IN;
IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR;
LS; LT; LU; LV; MA; MD; MG; MK; MN; MW;
MX; MZ; NA; NI; NO; NZ; OM; PG; PH; PL;
PT; RO; RU; SC; SD; SE; SG; SK; SL; SY;
TJ; TM; TN; TR; TT; TZ; UA; UG; US; UZ;
VC; VN; YU; ZA; ZM; ZW;

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PL; PT; RO; SE; SI; SK; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;

[AP] BW; GH; GM; KE; LS; MW; MZ; SD; SL; SZ;
TZ; UG; ZM; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 11880

Detailed Description:

...are available to the logical partitions according to the virtual processors defined for the respective logical partitions.

In one embodiment, the system 300 may operate in single machine partition (SMP) mode or in a logically partitioned (LPAR) mode. In a particular embodiment, a user of the system 300 may first be required... ...between partitions and other services. In another embodiment, primary and secondary partitions are not needed.

BILLING INFORMATION GENERATION AND VERIFICATION
Reference is now made again to FIGURE I to describe one...

14/3K/16 (Item 11 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

00870052
METHOD AND APPARATUS FOR CONTROLLING AN EXTENSIBLE COMPUTING SYSTEM
PROCEDE ET APPAREIL DE COMMANDE D'UN SYSTEME DE CALCUL EXTENSIBLE

Patent Applicant/Patent Assignee:

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US; US(Residence); US(Nationality)

Legal Representative:

s. BECKER Edward(et al)(agent)
Hickman Palermo Truong & Becker, LLP, 1600 Willow Street, San Jose, CA 95125; US;

	Country	Number	Kind	Date
Patent	WO	200203203	A2-A3	20020110
Application	WO	2001US19053		20010613
Priorities	US	2000213090		20000620
	US	2000630440		20000802

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; CH; CY; DE; DK; ES; FI; FR; GB;
GR; IE; IT; LU; MC; NL; PT; SE; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GW; ML;
MR; NE; SN; TD; TG;

[AP] GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ;
UG; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 17689

Detailed Description:

...control plane 902 is communicatively coupled to a global grid manager. Control plane 902 provides billing, fault, capacity, loading and other computing grid infonnation to the global grid manager. FIG. 13...
...global grid manager according to an embodiment.

In FIG. 13, a computing grid 1300 is partitioned into logical portions called grid segments 1302. Each grid segment 1302 includes a control plane 902 that...

NPL ABSTRACTS

10/5/1 (Item 1 from file: 2) Links
Fulltext available through: STIC Full Text Retrieval Options
INSPEC

08469293 INSPEC Abstract Number: C2003-01-6150N-059
Title: Using Virtual Linux servers
Author Norton, R.L.
Author Affiliation: Sch. of Comput. Sci. & Math., Marist Coll., Poughkeepsie, NY, USA
Journal: Computer vol.35, no.11 p. 106-7
Publisher: IEEE Comput. Soc ,
Publication Date: Nov. 2002 Country of Publication: USA
CODEN: CPTRB4 ISSN: 0018-9162
SICI: 0018-9162(200211)35:11L.106:UVLS;1-K
Material Identity Number: C125-2002-012
U.S. Copyright Clearance Center Code: 0018-9162/02/$17.00

Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: IBM has invested millions of dollars on Linux development and made the open-source operating system available on its entire server line. The company's recently announced Virtual Linux-On-Demand service will, for the first time, let companies access large-scale computing over the Internet. Instead of physical servers, customers will be able to tap into virtual servers on mainframes running Linux and be billed only for the computing power and resources they use. This will facilitate creation of e-utilities as well as help establish virtual organizations through grid technologies that enable rapid resource deployment. The paper considers how Marist College's School of Computer Science and Mathematics initiated a joint project with IBM built around using such servers. The college's IBM S/390 mainframe can run hundreds of Linux systems as virtual servers, all within a single logical partition.
Subfile: C
Descriptors: computer science education; IBM computers; Internet; network operating systems; Unix; virtual machines
Identifiers: Virtual Linux servers; open-source operating system; Marist College; computer science education; Virtual Linux-On-Demand service; Internet; virtual servers; virtual organizations; grid technologies; IBM S/390; mainframe
Class Codes: C6150N (Distributed systems software); C0220 (Computing education and training); C5620 (Computer networks and techniques)

1028069 ORDER NO: AAD13-33976
TECHNIQUES FOR MAPPING THE ALGORITHMS INTO THE HIGHER RADIX HYPERCUBE MULTIPROCESSORS

Author: GUPTA, PRAVEEN
Degree: M.S.
Year: 1988
Corporate Source/Institution: THE UNIVERSITY OF TEXAS AT ARLINGTON (2502)
SUPERVISOR: TSAIR-CHIN LIN
Source: Volume 27/01 of MASTERS ABSTRACTS. of Dissertations Abstracts International.
PAGE 119 . 66 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

The HIGHER RADIX HYPERCUBE (HRH) is investigated in this report as an interconnection network for multiprocessors. The HRH is based on a radix higher than two, the radix for the hypercube. We have compared several topological parameters for the HRH with the hypercube. It can be seen that HRH provides smaller diameter for a small price. A mapping and a partitioning algorithms are proposed for mapping different topologies to the HRH. In our mapping algorithm, we first map the problem topology to a virtual HRH, which is the most natural HRH for the problem. The virtual HRH is then transformed into the actual HRH. This algorithm is applicable to HRH used either as an interconnection or a virtual network. The partitioning algorithm reduces a large application topology to the required size by the iterative reduction process. Three examples of mapping topologies onto the HRH are also presented.

19/5/2 (Item 2 from file: 2) Links
INSPEC

06058578 INSPEC Abstract Number: C9511-6150N-025
Title: Architectural support for mobile objects in large scale distributed systems
Author Caughey, S.J.; Shrivastava, S.K.
Author Affiliation: Dept. of Comput. Sci., Newcastle upon Tyne Univ., UK
Conference Title: Proceeding. Fourth International Workshop on Object-Orientation in Operating Systems (IWOOOS '95) (Cat. No.95TH8120) p. 38-47
Editor(s): Cabrera, L.-F.; Theimer, M.
Publisher: IEEE Comput. Soc. Press , Los Alamitos, CA, USA
Publication Date: 1995 Country of Publication: USA ix+242 pp.
ISBN: 0 8186 7115 7
U.S. Copyright Clearance Center Code: 1063 5351/95/$04.00
Conference Title: Proceedings of International Workshop on Object Orientation in Operating Systems
Conference Sponsor: IEEE Comput. Soc.; IEEE Comput. Soc. Tech. Committee on Oper. Syst. & Application Environ.; Assoc. Int. Technol. Objets (AITO)
Conference Date: 14-15 Aug. 1995 Conference Location: Lund, Sweden

Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: The paper discusses the relevant features of an object support system that provides basic facilities for building flexible distributed applications in environments where objects can be mobile and occasional failures (node crashes, real or virtual network partitions) are possible. These facilities are for naming, locating and invoking objects, persistence and garbage collection. One of the key features is an efficient and reliable object reference scheme that is particularly good for dealing with mobile objects. The design presented scales to systems of arbitrary size and is portable since it only requires a few standard capabilities from the underlying operating system. (20 Refs)
Subfile: C
Descriptors: distributed processing; object-oriented programming; software fault tolerance
Identifiers: architectural support; mobile objects; large scale distributed systems; flexible distributed applications; node crashes; network partitions; persistence; garbage collection
Class Codes: C6150N (Distributed systems software); C6110J (Object-oriented programming)

19/5/3 (Item 3 from file: 2) Links
INSPEC

05687469 INSPEC Abstract Number: B9407-6210C-027, C9407-7410F-041
Title: The role of the Element Management Layer in network management
Author Aidarous, S.; Anderson, E.C.; Goett, J.M.; McGuire, E.D.R.; Mydosh, R.J.
Author Affiliation: Bell Northern Res. Ltd., Ottawa, Ont., Canada
Part vol.1 p. 59-69 vol.1
Publisher: IEEE , New York, NY, USA
Publication Date: 1994 Country of Publication: USA 3 vol. 964 pp.
ISBN: 0 7803 1811 0
U.S. Copyright Clearance Center Code: 0 7803 1811 0/94/$4.00
Conference Title: Proceedings of NOMS '94 - IEEE Network Operations and Management Symposium
Conference Sponsor: IEEE
Conference Date: 14-18 Feb. 1994 Conference Location: Kissimmee, FL, USA

Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Telecommunications Management Network (TMN) and related concepts have been a major focus of telecommunications operations work through the early 1990's. The emerging operations strategy is moving from the traditional OS-NE physical architecture to a multilayer model that is consistent with the ITU-T TMN Recommendation (M.3010) and that provides a logical partitioning that enables flexible physical placement alternatives. The purpose of this paper is to describe and provide a status readout of the work efforts on the Element Management Layer, one aspect of the multilayer model. The perspective given represents that of both Bellcore as agent of the Bell Regional Companies and that of a supplier. The paper begins by describing various networks that the EML program targets and the functional and logical architectures for EML applications that have been specified in Bellcore special reports. These are briefly reviewed. The paper then focuses on the emerging architectures and the impact that they will have on business services, operations, and technology within the Bell Regional Companies and the supplier community. Finally, a summary is given of what has been done, current status of Bell Regional Companies activities, and future work and challenges that must be addressed. (4 Refs)
Subfile: B C
Descriptors: telecommunication network management; telecommunications computer control
Identifiers: Element Management Layer; network management; Telecommunications Management Network; TMN; telecommunications operations; multilayer model; Bellcore; Bell Regional Companies; logical architectures; functional architectures; supplier community
Class Codes: B6210C (Network management); C7410F (Communications); C3370 (Communication techniques)

19/5/4 (Item 4 from file: 2) Links
INSPEC

03321099 INSPEC Abstract Number: C84047230
Title: Processing architecture evaluation simulation (PAES)
Author Schnaath, E.H.; Payne, H.J.
Author Affiliation: VERAC Inc., San Diego, CA, USA
Conference Title: Simulation in Strongly Typed Languages: ADA, PASCAL, SIMULA. Proceedings of the Conference p. 135-40
Editor(s): Bryant, R.; Unger, B.W.
Publisher: Soc. Comput. Simulation , La Jolla, CA, USA
Publication Date: 1984 Country of Publication: USA viii+167 pp.
Conference Sponsor: Soc. Comput. Simulation
Conference Date: 2-4 Feb. 1984 Conference Location: San Diego, CA, USA

Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A flexible tool for simulation of computer processing architectures has been designed, implemented, and used for analysis over a three-year period. This tool provides qualitative measures of processor and communications network performance. Provision for modular addition of processor operating systems and communication network protocols allows application-specific knowledge to be incorporated into the more general, application-independent, simulation framework. Modeling of candidate processing architecture performance evaluations have been generated for three distinct applications. Each hardware/software processing system evaluated is partitioned into four logical components: functional process specification from system level analysis; architecture definition; scenario description; and setting of simulation run parameters. This partitioning, in conjunction with interactive component entry and presentation of results, permits rapid model development and analysis. Implementing a single simulation in two programming languages, PASCAL and structured FORTRAN, has allowed a comparison of the effectiveness of each as a simulation implementation language. (9 Refs)
Subfile: C
Descriptors: computer architecture; digital simulation
Identifiers: evaluation; (PAES); simulation; computer processing architectures; communications network performance; PASCAL; structured FORTRAN
Class Codes: C5220 (Computer architecture); C7430 (Computer engineering)

19/5/5 (Item 1 from file: 8) Links
Ei Compendex(R)

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Title: A model of hierarchical real-time virtual resources

Author: Feng, Xiang Alex; Mok, Aloysius K.
Corporate Source: Department of Computer Sciences University of Texas at Austin, Austin, TX 78712, United States
Conference Title: Proceedings Real-Time Systems Symposium
Conference Location: Austin, TX, United States Conference Date: 20021203-20021205
Sponsor: IEEE Computer Society Technical Committee on Real-Time Systems
E.I. Conference No.: 60746
Source: Proceedings - Real-Time Systems Symposium 2002. p 26-35
Publication Year: 2002
CODEN: PRSYEA
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); X; (Experimental)
Journal Announcement: 0303W2
Abstract: A real-time virtual resource is an abstraction for resource sharing where application task groups must meet timing constraints and knowledge of all the timing requirements may not be available for a global schedulability analysis, such as is the case in the open system environment. In left bracket 12 right bracket , we introduced the notion of a real-time virtual resource which operates at a fraction of the rate of the shared physical resource and whose rate of service provision varies with time but is bounded. The shared resource is partitioned into real-time virtual resources by a resource-level scheduler such that each real-time virtual resource is accessible only by an individual application task group; tasks within the same task group are scheduled by an application-task-level scheduler that is specialized to the real-time requirements of the tasks in the group. In this paper, we propose a hierarchical real-time virtual resource model that permits resource partitioning to be extended to multiple levels. Through this model, partitions on each level are scheduled as if they had access to a dedicated resource and there is minimal interference between neighboring partition levels. We also investigate the partitioning of real-time virtual resources subject to scheduling quantum requirements. 16 Refs.
Descriptors: *Real time systems; Virtual reality; Computer simulation; Resource allocation; Open systems; Constraint theory; Response time (computer systems); Computer operating systems; Algorithms; Theorem proving
Identifiers: Real time virtual resources; Resource partition; Resource sharing; Real time scheduling; Scheduling quantum; Timing constraints
Classification Codes:
722.4 (Digital Computers & Systems); 723.5 (Computer Applications); 912.2 (Management); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory)); 723.1 (Computer Programming)
722 (Computer Hardware); 723 (Computer Software, Data Handling & Applications); 912 (Industrial Engineering & Management); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

19/5/8 (Item 3 from file: 23) Links
CSA Technology Research Database

0004807201 IP Accession No: 0169684
MVS/ESA full vs. reduced/partial preemption

Lambourne, Steve Hitachi Data Systems Corp
Pages: 1347-1352
Publication Date: 1994
Publisher: CMG, CHICAGO, IL, (USA)

Conference:
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Document Type: Conference Paper
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Language: English
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Abstract:
This paper concerns itself with changes made to the MVS dispatcher. The changes were introduced with MVS/ESA and refined in subsequent releases of MVS/ESA. Architectural issues such as MP exploitation, SIGP processing, processor speeds, and LPAR environments may all have contributed to the need for redesign of the MVS/ESA dispatcher.

Descriptors: Computer architecture; Digital computers; Computational methods; Buffer circuits; Computer operating procedures; Computer hardware; Computer software; Data storage equipment
Identifiers: MVS/ESA operating system; MP exploitation; Signal processor processing; Processor speeds; Mainframes; High speed buffer; Hardware overhead; Software overhead
Subj Catg: C 723, Computer Software, Data Handling and Applications; C 722, Computer Hardware; C 722.4, Digital Computers and Systems; C 721.1, Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); C 722.1, Data Storage (Equipment and Techniques)

19/5/9 (Item 1 from file: 35) Links
Dissertation Abs Online

01974300 ORDER NO: AADAA-I3105239
System architecture for wireless sensor networks

Author: Hill, Jason Lester
Degree: Ph.D.
Year: 2003
Corporate Source/Institution: University of California, Berkeley (0028)
Adviser: David E. Culler
Source: Volume 6409B of Dissertations Abstracts International.
PAGE 4458 . 186 PAGES
Descriptors: COMPUTER SCIENCE ; ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0984; 0544

In this thesis we present and operating system and three generations of a hardware platform designed to address the needs of wireless sensor networks. Our operating system, called TinyOS uses an event based execution model to provide support for fine-grained concurrency and incorporates a highly efficient component model. TinyOS enables us to use a hardware architecture that has a single processor time shared between both application and protocol processing. We show how a virtual partitioning of computational resources not only leads to efficient resource utilization but allows for a rich interface between application and protocol processing. This rich interface, in turn, allows developers to exploit application specific communication protocols that significantly improve system performance.

The hardware platforms we develop are used to validate a generalized architecture that is technology independent. Our general architecture contains a single central controller that performs both application and protocol-level processing. For flexibility, this controller is directly connected to the RF transceiver. For efficiency, the controller is supported by a collection of hardware accelerators that provide basic communication primitives that can be flexibility composed into application specific protocols.

The three hardware platforms we present are instances of this general architecture with varying degrees of hardware sophistication. The Rene platform serves as a baseline and does not contain any hardware accelerators. It allows us to develop the TinyOS operating system concepts and refine its concurrency mechanisms. The Mica node incorporates hardware accelerators that improve communication rates and synchronization accuracy within the constraints of current microcontrollers. As an approximation of our general architecture, we use Mica to validate the underlying architectural principles. The Mica platform has become the foundation for hundreds of wireless sensor network research efforts around the world. It has been sold to more than 250 organizations.

Spec is the most advanced node presented and represents the full realization of our general architecture. It is a 2.5 mm x 2.5 mm CMOS chip that includes processing, storage, wireless communications and hardware accelerators. We show how the careful selection of the correct accelerators can lead to orders-of-magnitude improvements in efficiency without sacrificing flexibility. In addition to performing a theoretical analysis on the strengths of our architecture, we demonstrate its capabilities through a collection of real-world application deployments.